I input port mechanisms with a width, which receive packets having data from a communication line, where I is greater than or equal to 1 and is an integer;

O output port mechanisms with a width, which send packets to a communication line, where O is greater than or equal to 1 and is an integer;

a carrier mechanism for carrying packets in an allocated time slot, said carrier mechanism having a width wider than the width of the input and output port mechanisms so data from more than one packet at a time is transferred in the allocated time slot, said carrier mechanism connected to each input port mechanism and each output port mechanism;

a memory mechanism in which packets are stored, said memory mechanism connected to the carrier mechanism; and

a mechanism for providing data from more than one packet at a time to the memory mechanism through the carrier mechanism from the input port mechanisms, the providing mechanism includes input stage queue groups connected to the carrier mechanism and the input port mechanisms for storing packets received by the input port mechanisms, and output stage queue groups connected to the providing mechanism and the output port mechanisms for storing packets to be sent out the output port mechanisms, said providing

mechanism transferring more than one packet at a time in the allocated time slot whose total width equals the width of the carrier mechanism in each allocated time slot to the memory mechanism, said providing mechanism transferring more than one packet at a time to the memory mechanism in the allocated time slot only when there is enough data from more than one packet from an input stage queue group to fill the width but not transferring any data from any packets from the input stage queue group in the allocated time slot when there is not enough data to fill the width of the carrier mechanism.

C1

Cancel Claim 6.

7. A system as described in Claim 5 wherein the providing mechanism includes a classifying mechanism which places a packet which is received by the input port mechanism into a corresponding queue group, said classifying mechanism connected to the input port mechanisms and the input stage queue groups.

C2

15. A switching system for packets comprising:

a central resource having a width and an overall bandwidth and input port mechanisms and output port mechanisms each having widths for receiving or sending packets, respectively, said central resource partitioned via time slots that are allocated to the input and

C3

output port mechanisms, said central resource width independent of any input or output port mechanisms width and the overall bandwidth can grow without limitation by the input or output port mechanisms width; and

C3

a memory mechanism for storing packets, said memory mechanism connected to the central resource and receiving more than one packet at a time in a respective time slot from the central resource which completely fills the width of the central resource, the central resource transferring more than one packet at a time to the memory mechanism in the respective time slot only when there is enough data from more than one packet to fill the total width but not transferring any data from any packets in the respective time slot when there is not enough data to fill the total width of the carrier mechanism.

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18. A switching system comprising:

C4

a time division multiplex bus having a width;

a memory mechanism connected to the bus which is accessed via time slots in time division multiplexing of the bus; and

a mechanism for reading and writing data of packets to the memory mechanism through the bus without knowledge of the packet boundaries of the data, the reading and writing mechanism transferring more than one packet at a time to or from the memory mechanism in a respective time slot only when there is enough data from more than one packet to fill the width but not transferring any data from any packets in the respective time slot when there is not enough data to fill the width of the bus.

19. A switching system comprising:

a time division multiplex carrier mechanism having a width;

a memory mechanism connected to the carrier mechanism which is accessed via time slots in time division multiplexing of the bus; and

an input stage mechanism having a width for providing data of packets to the memory mechanism so the data of the packets fills the width of the bus via time division multiplexing, said bus width a positive non-integer multiple of the input stage mechanism width a mechanism for providing data of packets having a width to the memory mechanism so the data of the packets fills the width of the bus via time division multiplexing, said bus width a positive non-integer multiple of the packet width greater than one, the input stage mechanism

transferring more than one packet at a time to the memory mechanism in a respective time slot only when there is enough data from more than one packet to fill the width but not transferring any data from any packets in the respective time slot when there is not enough data to fill the width of the carrier mechanism.

20. A method for switching packets having a width comprising the steps of:

receiving a first packet and at least a second packet at a switch mechanism; and

C4

transferring data of the first packet and the second packet to a memory mechanism via time slots in time division multiplexing of a bus having a width only when data from the packets fills a predetermined portion of the width of the bus in a time slot, but not transferring any data from the first and second packets in the time slot when there is not enough data to fill the predetermined portion of the width of the bus, said bus width not a function of the data contained in any packet.

Please add the following claim.

25. A system as described in Claim 14 wherein the memory mechanism has

C5

packets stored in it without knowledge of the packet boundaries of the packets.